CLAIMS

What is claimed is:

1. A phase-locked loop (PLL) circuit, comprising:

a voltage-controlled oscillator (VCO) having a first input to receive a control voltage, one or more second inputs to receive one or more tuning range control signals, and an output to provide an oscillation output signal;

a phase detector having inputs to receive the oscillation output signal and a reference signal, and having an output;

a charge pump having an input coupled to the output of the phase detector and having an output to generate the control voltage;

a loop filter having an input to receive the control voltage and having a control terminal; and

a controller having inputs to receive the control voltage, a high reference voltage, a low reference voltage, and one or more mode signals, and having a first output connected to the control terminal of the loop filter and second outputs to generate the tuning range signals.

2. The PLL circuit of Claim 1, wherein the one or more tuning range signals select one of a plurality of tuning ranges for the VCO.

3. The PLL circuit of Claim 1, wherein the mode signals are set to a first state to allow the controller to automatically generate the one or more tuning range signals.

4. The PLL circuit of Claim 3, wherein the one or more tuning range signals are generated in response to comparisons between the control voltage and the reference voltages.

5. The PLL circuit of Claim 4, wherein the one or more tuning range signals instruct the VCO to select a higher tuning range if the control voltage is greater than the high reference voltage.

6. The PLL circuit of Claim 4, wherein the one or more tuning range signals instruct the VCO to select a lower tuning range if the control voltage is less than the low reference voltage.

7. The PLL circuit of Claim 3, wherein the mode signals are set to a second state and control the one or more tuning range signals.

8. The PLL circuit of Claim 7, wherein the mode signals are generated externally and provided as input signals to the PLL circuit.

9. The PLL circuit of Claim 1, wherein the VCO comprises a differential oscillator circuit having:

a first transistor coupled between a first output terminal and a bias node, and having a gate coupled to a second output terminal;

a second transistor coupled between the second output terminal and the bias node, and having a gate coupled to the first output terminal; and

a resonant circuit coupled between the first and second output terminals, and comprising:

an offset capacitor coupled between the first and second output terminals;

a first capacitor and a first switch connected in series between the first and second output terminals, the first switch controlled by a first tuning range control signal;

a second capacitor and a second switch connected in series between the first and second output terminals, the second switch controlled by a second tuning range control signal; and

a varactor coupled between the first and second output terminals, the varactor including a terminal to receive the control voltage.

10. The PLL circuit of Claim 9, wherein the differential oscillator circuit further comprises:

a third transistor connected in parallel with the first transistor and having a gate to receive a first input signal; and

a fourth transistor connected in parallel with the second transistor and having a gate to receive a second input signal.

11. The PLL circuit of Claim 10, wherein the first and second input signals are 180 degrees out of phase.

12. The PLL circuit of Claim 10, wherein the VCO further comprises two of the differential oscillator circuits connected in a cascade configuration to provide a four-phase oscillation output.

13. The PLL circuit of Claim 1, wherein the controller comprises:

a comparator circuit having a first input to receive the

high reference voltage, a second input to receive the low reference voltage, a third input to receive a middle reference voltage, and outputs to generate a plurality of corresponding compare signals; and

a finite state machine having first inputs to receive the compare signals, and first outputs to generate the one or more tuning range control signals in response to the compare signals.

14. The PLL circuit of Claim 13, wherein the control terminal of the loop filter is configured to receive a reset signal generated by the finite state machine.

15. The PLL circuit of Claim 14, wherein assertion of the reset signal causes the loop filter to reset the control voltage to a predetermined value.

16. The PLL circuit of Claim 14, wherein the reset signal is asserted in response to a change in the tuning range control signals.

17. The PLL circuit of Claim 13, wherein the comparator comprises hysteresis.

18. The PLL circuit of Claim 13, wherein the controller further comprises:

a counter having inputs coupled to the first outputs of the finite state machine, and an output to generate a counter signal;

a multiplexer having a first input to receive the counter signal, a second input to receive the one or more mode signals, a control terminal to receive a logic combination of the one or

more mode signals, and an output to provide the tuning range signals to the VCO.

19. The PLL circuit of Claim 18, wherein the controller further comprises:

a decoder coupled between the multiplexer output and the VCO.

20. The PLL circuit of Claim 1, wherein one or more of the tuning ranges overlaps an adjacent tuning range.

21. A phase-locked loop (PLL) circuit, comprising:

a voltage-controlled oscillator (VCO) having a first input to receive a control voltage, a second input to receive a tuning range control signal that configures the VCO to one of a plurality of adjacent tuning ranges, and an output to provide an oscillation output signal;

a phase detector having inputs to receive the oscillation output signal and a reference signal, and having an output;

a charge pump and loop filter circuit having an input coupled to the output of the phase detector, an output to generate the control voltage, and a control terminal to receive a reset signal; and

a controller for generating the tuning range control signal and the reset signal in response to a plurality of reference voltages and a mode signal.

22. The PLL circuit of Claim 21, wherein the mode signal selects whether the VCO automatically select one of the tuning ranges or whether an externally generated signal instructs the VCO to select one of the tuning ranges.

23. The PLL circuit of Claim 21, wherein setting the mode signal to a first state configures the controller to adjust the tuning range control signal in response to a comparison between the control voltage and the plurality of reference voltages.

24. The PLL circuit of Claim 23, wherein setting the mode signal to a second state configures the controller to adjust the tuning range control signal in response to the mode signal.

25. The PLL circuit of Claim 24, wherein the mode signal is generated externally and provided as an input signal to the PLL circuit.

26. The PLL circuit of Claim 21, wherein the charge pump and loop filter circuit selectively resets the control voltage to a predetermined voltage in response to the reset signal.

27. The PLL circuit of Claim 21, wherein the controller comprises:

a comparator circuit having a first input to receive a high reference voltage, a second input to receive a low reference voltage, a third input to receive a middle reference voltage, and outputs to generate a plurality of corresponding compare signals;

a finite state machine having first inputs to receive the compare signals, having first outputs to generate a shift up signal and a shift down signal, and having a second output to generate the reset signal;

a counter having inputs to receive the shift up and shift down signals, and having an output to generate a counter signal;

and

a multiplexer having a first input to receive the counter signal, a second input to receive the mode signal, a control terminal to receive a select signal, and an output to provide the tuning range signal to the VCO.

28. The PLL circuit of Claim 27, wherein the select signal comprises the mode signal.

29. The PLL circuit of Claim 27, wherein the controller further comprises:

a decoder coupled between the multiplexer output and the VCO.

30. The PLL circuit of Claim 21, wherein the VCO comprises a differential oscillator circuit having:

a first transistor coupled between a first output terminal and a bias node, and having a gate coupled to a second output terminal;

a second transistor coupled between the second output terminal and the bias node, and having a gate coupled to the first output terminal; and

a resonant circuit coupled between the first and second output terminals, and comprising:

an offset capacitor coupled between the first and second output terminals;

a first capacitor and a first switch connected in series between the first and second output terminals, the first switch controlled by a first tuning range control signal;

a second capacitor and a second switch connected in

series between the first and second output terminals, the second switch controlled by a second tuning range control signal; and

a varactor coupled between the first and second output terminals, the varactor including a terminal to receive the control voltage.

31. The PLL circuit of Claim 30, wherein the differential oscillator circuit further comprises:

a third transistor connected in parallel with the first transistor and having a gate to receive a first input signal; and

a fourth transistor connected in parallel with the second transistor and having a gate to receive a second input signal.

32. The PLL circuit of Claim 31, wherein the first and second input signals are 180 degrees out of phase.

33. The PLL circuit of Claim 31, wherein the VCO further comprises two of the differential oscillator circuits connected in a cascade configuration to provide a four-phase oscillation output.

34. A method of operating a phase-locked loop (PLL) circuit having a plurality of substantially adjacent frequency tuning ranges, comprising:

configuring the circuit to initially operate in a selected frequency tuning range;

generating an oscillation output signal;

comparing the oscillation output signal with a reference signal to generate a control voltage;

comparing the control voltage to first and second reference voltages to generate a compare signal, wherein the first reference voltage is less than the second reference voltage;

selectively changing the frequency tuning range in response to the compare signal.

35. The method of Claim 34, wherein the selectively changing further comprises:

selecting a lower frequency tuning range if the control voltage is less than the first reference voltage;

selecting a higher frequency tuning range if the control voltage is greater than the second reference voltage; and

locking the selected frequency tuning range if the control voltage is between the first and second reference voltages.

36. The method of Claim 35, further comprising:

asserting a reset signal if the frequency tuning range is changed; and

resetting the control voltage to a predetermined value in response to the reset signal.

37. The method of Claim 35, further comprising:

providing a mode signal to the circuit;

allowing the circuit to automatically select a frequency tuning range if the mode signal is in a first state; and

instructing the circuit to select a particular frequency tuning range indicated by the mode signal if the mode signal is in a second state.

38. The method of Claim 34, wherein the selectively changing further comprises:

asserting a shift-up signal if the control voltage is less than the first reference voltage;

asserting a shift-down signal if the control voltage is greater than the second reference voltage;

incrementing a counter value in response to the shift-up and shift-down signals;

generating a tuning range control signal in response to the counter value; and

adjusting the frequency tuning range in response to the tuning range control signal.

39. The method of Claim 38, wherein the selectively changing further comprises:

providing an externally generated mode signal;

generating the tuning range control signal in response to the counter value if the mode control signal is in a first state; and

generating the tuning range control signal in response to the mode signal if the mode signal is in a second state.